

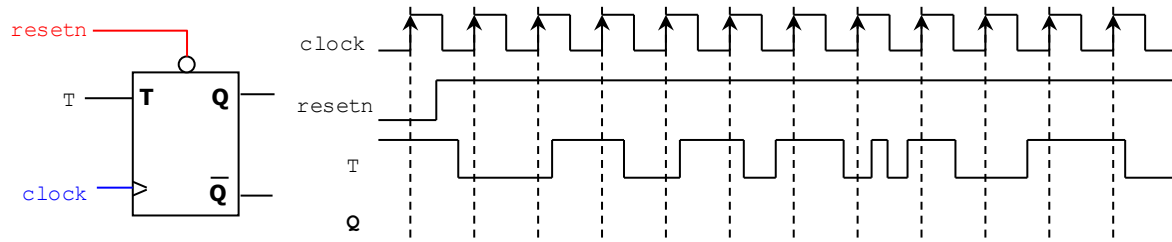
Homework 3

(Due date: October 31st @ 5:30 pm)

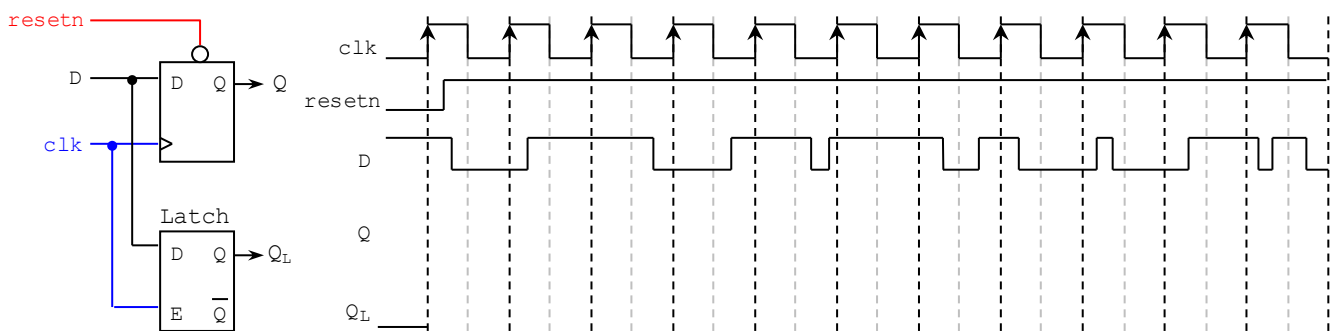
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (12 PTS)

- Complete the timing diagram of the circuit shown below. (5 pts)

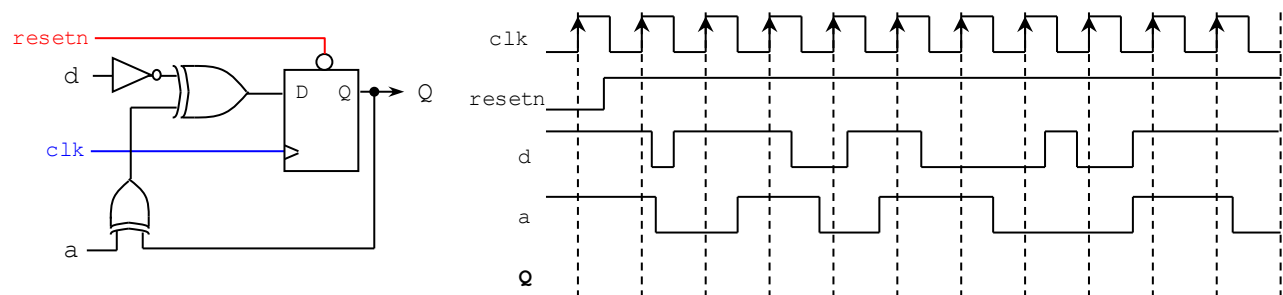


- Complete the timing diagram of the circuits shown below: (7 pts)

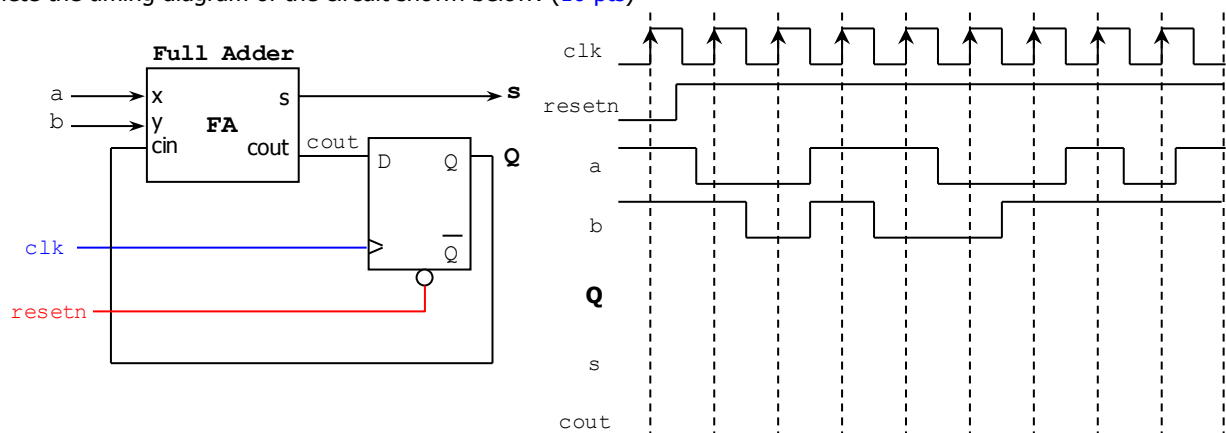


PROBLEM 2 (17 PTS)

- Complete the timing diagram of the circuit shown below: (7 pts)



- Complete the timing diagram of the circuit shown below: (10 pts)



PROBLEM 3 (16 PTS)

- With a D flip flop and logic gates, sketch the circuit whose excitation equation is given by:

$$q(t+1) \leftarrow \bar{x}y + \bar{x}q(t) + yq(t) \quad (4 \text{ pts})$$
- Complete the timing diagram of the circuit whose VHDL description is shown below. Also, get the excitation equation for q .

```

library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port (clrn, clk, a: in std_logic;
        q: out std_logic);
end circ;

architecture t of circ is
  signal qt: std_logic;

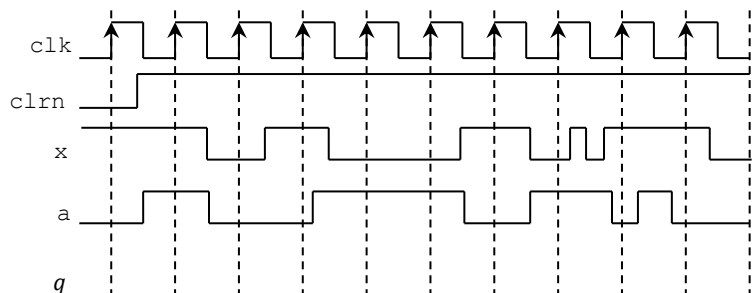
begin
  process (clrn, clk, x, a)
  begin
    if clrn = '0' then
      qt <= '0';
    end if;
  end process;
end t;

```

```

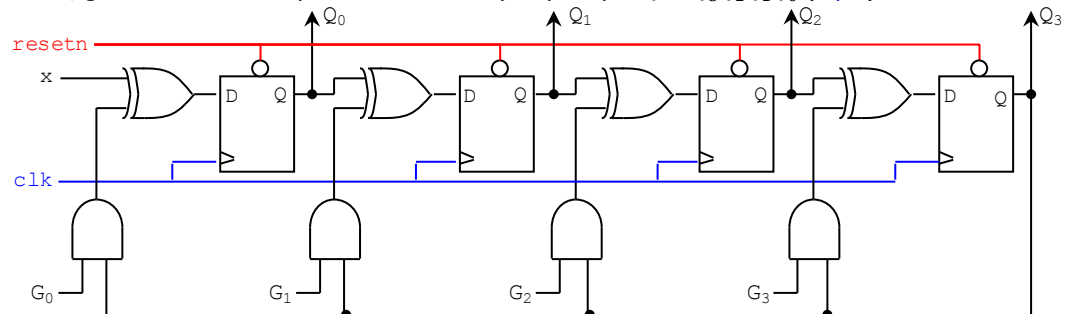
elsif (clk'event and clk = '1') then
  if x = '1' then
    qt <= a xor not(qt);
  end if;
end if;
end process;
q <= qt;
end t;

```



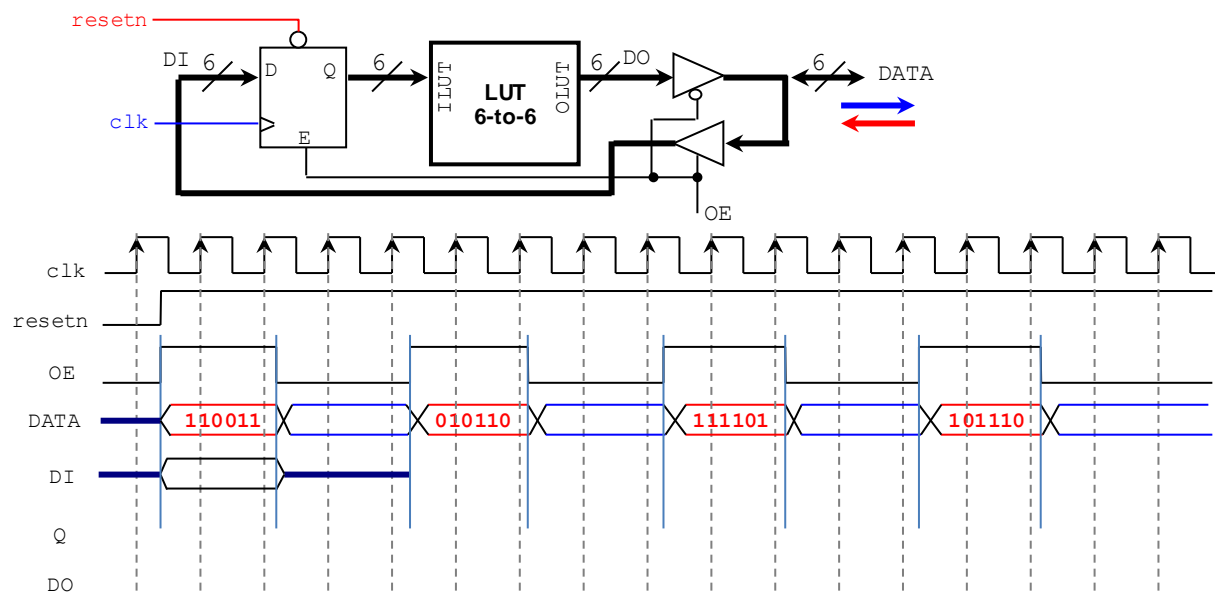
$$q(t+1) \leftarrow$$

- Given the following circuit, get the excitation equations for each flip flop output $Q = Q_3Q_2Q_1Q_0$ (6 pts)



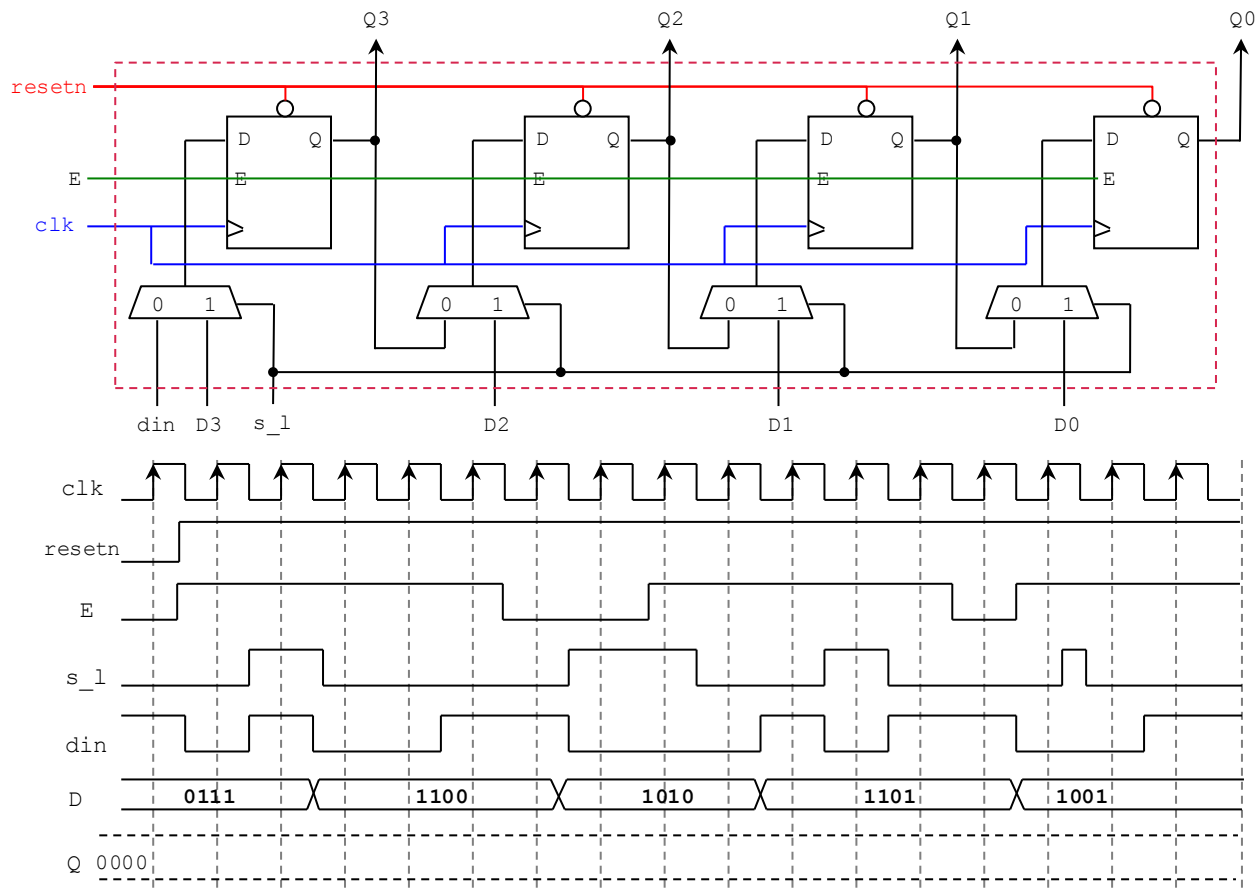
PROBLEM 4 (18 PTS)

- Given the following circuit, complete the timing diagram (signals DO , Q and $DATA$).
 The LUT 6-to-6 implements the following function: $OLUT = [ILUT^{0.85}]$, where $ILUT$ is an unsigned number.
 For example $ILUT = 35 (100011_2) \rightarrow OLUT = \lceil 35^{0.85} \rceil = 21 (010101_2)$



PROBLEM 5 (12 PTS)

- Complete the timing diagram of the following 4-bit parallel access shift register with enable input. Shifting operation: $s_1=0$. Parallel load: $s_1=1$. Note that $Q = Q_3Q_2Q_1Q_0$. $D = D_3D_2D_1D_0$



PROBLEM 6 (25 PTS)

- The following circuit is a multiple-input compressor circuit (MIC), a component in Built-in Self-Test systems. $Q = Q_3Q_2Q_1Q_0$. $P = P_3P_2P_1P_0$
 - Write structural VHDL code. Create two files: i) flip flop, ii) top file (where you will interconnect the flip flops and the logic gates). Provide a printout. (10 pts)
 - Write a VHDL testbench according to the timing diagram shown below. Complete the timing diagram by simulating your circuit (Behavioral Simulation). The clock frequency must be 100 MHz with 50% duty cycle. Provide a printout. (15 pts)

